

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	50	("5021963" "5241672" "5726894" "6502240" "6668336" "6883114" "4528644" "4578774" "4783745" "4837714" "6591389" "6850973" "5260900" "5502813" "5696730" "6083791" "6134156" "6137421" "6421276" "4424573" "4442501" "4534018" "4584647" "4627016" "4802117" "4809185" "4813912" "4858138" "4901273" "4922456" "4947410" "5218569" "5263152" "5269019" "5377264" "5394362" "5433537" "5438519" "5438844" "5511020" "5526741" "5559579" "5566344" "5581779" "5598573" "5606710" "5613144" "5623686" "5628199" "5651103").pn.	US-PGPUB; USPAT	OR	ON	2005/12/11 14:14
L2	22866637	@ad<"20020905"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:14
L3	50	1 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:15
L4	444349	eeeprom or eprom or prom or e2prom or (nonvolatile adj memory) or (non-volatile adj memory) or flash	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:16
L5	404249	updat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:16
L6	8813	4 with 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:16
L7	2567580	compare or compared or comparison	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:17
L8	590	6 same 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:17
L9	213259	previous and original	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:18

L10	31	8 same previous	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:18
L11	16	8 same original	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:18
L12	0	10 and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:18
L13	47	10 or 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:19
L14	0	1 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:19
L15	34	2 and 13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:24
L16	2	"6523083".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:24
L17	7	("5603056" "5819108" "5901330" "6009497" "6038640" "6151657" "6253281").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:25
L18	8	16 or 17	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:25
L19	0	13 and 18	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:25
L20	0	8 and 18	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:25
L21	1	1 and 8	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:26
L22	12	1 and 6	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:27
L23	1474	711/103.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:27

L24	637	711/115.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:27
L25	2032	711/154.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:27
L26	1202	711/163.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:27
L27	1913	711/170.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:27
L28	6371	23 or 24 or 25 or 26 or 27	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:27
L29	178000	"710"/("8,10,11").ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:28
L30	1301	710/8.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:28
L31	710	710/10.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:28
L32	162	710/13.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:28
L33	1870	30 or 31 or 32	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:28
L34	1841	713/1.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:28
L35	1023	713/100.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:28
L36	2456	34 or 35	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:29
L37	3086405	28 or 33 or 36	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:29
L38	10126	28 or 33 or 36	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:29
L39	59	8 and 38	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:29
L40	45	2 and 39	US-PGPUB; USPAT; USOCR	OR	ON	2005/12/11 14:31

L41	4	13 and 40	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/11 14:33
L42	547	711/103.ccls.	US-PGPUB	OR	ON	2005/12/11 14:34
L43	214	2 and 42	US-PGPUB	OR	ON	2005/12/11 14:34
L44	5	8 and 43	US-PGPUB	OR	ON	2005/12/11 14:34



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Kosaka, H.; Shibata, T.; Ishii, H.; Ohmi, T.;
Electron Devices, IEEE Transactions on
Volume 42, Issue 1, Jan. 1995 Page(s):135 - 143
Digital Object Identifier 10.1109/16.370025
[AbstractPlus](#) | Full Text: [PDF\(676 KB\)](#) IEEE JNL
- ☐ 2. **Mapping structures for flash memories: techniques and open problems**
Gal, E.; Toledo, S.;
Software - Science, Technology and Engineering, 2005. Proceedings. IEEE International Conference on
22-23 Feb. 2005 Page(s):83 - 92
Digital Object Identifier 10.1109/SWSTE.2005.14
[AbstractPlus](#) | Full Text: [PDF\(152 KB\)](#) IEEE CNF
- ☐ 3. **Reliability model and Implementation for EEPROM emulation using flash memory**
Chen He; Kuhn, P.; Jew, T.; Niset, M.;
Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International
25-29 April 2004 Page(s):657 - 658
[AbstractPlus](#) | Full Text: [PDF\(252 KB\)](#) IEEE CNF
- ☐ 4. **Process qualification strategy for advanced embedded non-volatile memory technology - the Philips 0.18 /spl mu/m embedded flash case**
Guoqiao Tao; Scarpa, A.; van Dijk, K.; Kuper, F.G.;
Reliability Physics Symposium Proceedings, 2003. 41st Annual. 2003 IEEE International
30 March-4 April 2003 Page(s):604 - 605
Digital Object Identifier 10.1109/RELPHY.2003.1197827
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IEE JNL IEE Journal or Magazine










IEEE CNF IEEE Conference Proceeding

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IEEE STD IEEE Standard

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- ☐ 1. **Testing and remote field update of distributed base stations in a wireless network**
Chen-Huan Chiang; Wheatley, P.J.; Ho, K.Y.; Cheung, K.L.;
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26-28 Oct. 2004 Page(s):711 - 718
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- ☐ 2. **Flash memory BIOS for PC and notebook computers**
Jex, J.;
Communications, Computers and Signal Processing, 1991., IEEE Pacific Rim Conference on
9-10 May 1991 Page(s):692 - 695 vol.2
Digital Object Identifier 10.1109/PACRIM.1991.160834
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- ☐ 3. **An excellent weight-updating-linearity EEPROM synapse memory cell for self-learning Neuron-MOS neural networks**
Kosaka, H.; Shibata, T.; Ishii, H.; Ohmi, T.;
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- ☐ 4. **A single-transistor silicon synapse**
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Morie, T.; Fujita, O.; Uchimura, K.;
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- ☐ 6. **Hardware-supported asynchronous checkpointing scheme**
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-  9. **Reliability model and implementation for EEPROM emulation using flash memory**
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-  10. **An excellent weight-updating-linearity synapse memory cell for self-learning neuron MOS neural networks**
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-  11. **Custom design of a hardware fuzzy logic controller**
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-  12. **A neuron-MOS neural network using self-learning-compatible synapse circuits**
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-  13. **Mapping structures for flash memories: techniques and open problems**
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-  14. **Adaptive ANN rule-based controller for a chopper fed PMDC motor electric vehicles drive**
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16. Process qualification strategy for advanced embedded non-volatile memory technology - the Philips 0.18 μm /m embedded flash case

Guoqiao Tao; Scarpa, A.; van Dijk, K.; Kuper, F.G.;

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30 March-4 April 2003 Page(s):604 - 605

Digital Object Identifier 10.1109/RELPHY.2003.1197827

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